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In the Claims:

1-7. (Cancelled)

8. (Currently Amended) A method for controlling accuracy and repeatability of an etch process, comprising:

(a) providing a batch of substrates, each substrate having a patterned mask formed on a film stack comprising at least one material layer;

(b) measuring dimensions of elements of the patterned mask on at least one substrate of the batch of substrates;

(c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b);

(d) etching the at least one material layer on the at least one substrate;

(e) at least one of compacting or removing at least a portion of post-etch residue formed on sidewalls of the etched structures;

(e) (f) measuring dimensions of etched structures formed on the at least one substrate during step (d); and

(f) (g) adjusting the process recipe of step (c) or/and the process recipe of step (d) based on the measurements performed at step (e) (f).

9. (Currently Amended) The method of claim 8 wherein the steps (b) and (e) (f) use an optical measuring technique.

10. (Original) The method of claim 9 wherein the optical measuring technique is a scatterometric measuring technique.

11. (Currently Amended) The method of claim 8 wherein the steps (b) through (e) (f) are performed using processing modules of a single substrate processing system.

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12. (Currently Amended) The method of claim 8 wherein the step (f) (g) further comprises:

modifying a time duration or process parameters for trimming the patterned mask.

13. (Currently Amended) The method of claim 8 wherein the step (f) (g) further comprises:

modifying a time duration or process parameters for etching the material layer.

14. (Cancelled)

15. (Currently Amended) The method of claim 14 claim 8 further comprising:
thinning the post-etch residue to a thickness of less than about 10 nm.

16. (Currently Amended) A method for controlling accuracy and repeatability during formation of a gate structure of a field effect transistor, comprising:

(a) providing a batch of substrates, each substrate having a patterned mask formed on a gate electrode layer of the gate structure;

(b) measuring dimensions of elements of the patterned mask on at least one substrate of the batch of substrates;

(c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b);

(d) etching the gate electrode layer on the at least one substrate;

(e) at least one of compacting or removing at least a portion of post-etch residue formed on sidewalls of the etched structures;

(e) (f) measuring dimensions of etched gate electrode structures formed on the at least one substrate during step (d); and

(f) (g) adjusting the process recipe of step (c) or/and the process recipe of step (d) based on the measurements performed at step (e) (f).

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PAGE 4/10 * RCVD AT 9/28/2005 2:47:11 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/32 * DNIS:2738300 * CSID:732 530 9808 * DURATION (mm:ss):02-20

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17. (Currently Amended) The method of claim 16 wherein the steps (b) and (e) (f) use an optical measuring technique.

18. (Previously Presented) The method of claim 17 wherein the optical measuring technique is a scatterometric measuring technique.

19. (Currently Amended) The method of claim 16 wherein the steps (b) through (e) (f) are performed using processing modules of a single substrate processing system.

20. (Currently Amended) The method of claim 16 wherein the step (f) (g) further comprises:

modifying a time duration or process parameters for trimming the patterned mask.

21. (Currently Amended) The method of claim 16 wherein the step (f) (g) further comprises:

modifying a time duration or process parameters for etching the material layer.

22. (Previously Presented) The method of claim 16 wherein the gate electrode layer comprises doped polysilicon.

23. (Previously Presented) The method of claim 16 wherein the step (d) further comprises:

providing HBr and Cl₂ at a flow ratio HBr:Cl₂ in a range from 1:15 to 15:1.

24. (Cancelled)

25. (Currently Amended) The method of ~~claim 24~~ claim 16 further comprising:
thinning the post-etch residue to a thickness of less than about 10 nm.

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26. (Previously Presented) The method of claim 23 further comprising:
using a plasma comprising one or more gases selected from the group
consisting of nitrogen (N₂), oxygen (O₂) and hydrogen (H₂).

27. (Currently Amended) The method of claim 26 further comprising:
providing nitrogen (N₂) and hydrogen (H₂) at a N₂:H₂ flow ratio in a range from
3:1 to 100% of N₂;
maintaining the substrate at a temperature between about 200 and 350 degrees
Celsius;
applying power to an inductively coupled power source between about 1000 and
7000 W; and
maintaining a chamber pressure between about 500 and 2000 mTorr.

28-30. (Cancelled)

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